```
     FILE 'REGISTRY' ENTERED AT 08:46:35 ON 10 MAR 2005
L17           40 SEA ABB=ON  PLU=ON  B/MF
L18         1420 SEA ABB=ON  PLU=ON  B.N/MF OR B N/ELF
L19          227 SEA ABB=ON  PLU=ON  W/MF
L20          152 SEA ABB=ON  PLU=ON  N.W/MF OR N W/ELF
L21           25 SEA ABB=ON  PLU=ON  B N W/ELF
L22           33 SEA ABB=ON  PLU=ON  B.N.W/MF

     FILE 'HCAPLUS' ENTERED AT 08:47:42 ON 10 MAR 2005

L23            1 SEA ABB=ON  PLU=ON  US6863727/PN
L24            2 SEA ABB=ON  PLU=ON  US20040142557/PN
L25            3 SEA ABB=ON  PLU=ON  (L23 OR L24)
L26              SEL PLU=ON  L25 1- RN :      108 TERMS

     FILE 'REGISTRY' ENTERED AT 08:49:00 ON 10 MAR 2005
L27          108 SEA ABB=ON  PLU=ON  L26
L28           37 SEA ABB=ON  PLU=ON  L27 AND B/MAC,ELS

     FILE 'REGISTRY' ENTERED AT 08:49:06 ON 10 MAR 2005
L29          108 SEA ABB=ON  PLU=ON  L26
L30           31 SEA ABB=ON  PLU=ON  L29 AND W/MAC,ELS

     FILE 'REGISTRY' ENTERED AT 08:49:19 ON 10 MAR 2005
L31          108 SEA ABB=ON  PLU=ON  L26
L32           20 SEA ABB=ON  PLU=ON  L31 AND N/MAC,ELS

     FILE 'STNGUIDE' ENTERED AT 08:49:48 ON 10 MAR 2005

     FILE 'REGISTRY' ENTERED AT 09:07:39 ON 10 MAR 2005
L33         2956 SEA ABB=ON  PLU=ON  B H/ELF OR B.H/MF
                 E C H B/MF
L34            6 SEA ABB=ON  PLU=ON  "C H B"/MF
                 E C H B/ELF
L35        26862 SEA ABB=ON  PLU=ON  "C H B"/ELF

     FILE 'HCAPLUS' ENTERED AT 09:11:27 ON 10 MAR 2005
L36         5842 SEA ABB=ON  PLU=ON  ((L17 OR L18) OR (L21 OR L22) OR L28 OR
                 (L33 OR L34 OR L35)) AND ((L19 OR L20 OR L21 OR L22) OR WN OR
                 TUNGSTEN NITRIDE OR W NITRIDE)
L37         4006 SEA ABB=ON  PLU=ON  FIRST(3A)(B OR BORON)
L38            6 SEA ABB=ON  PLU=ON  L36 AND L37
L39        14666 SEA ABB=ON  PLU=ON  SUBSTRATE(5A)(B OR BORON)
L40        12109 SEA ABB=ON  PLU=ON  LOWER(5A)(B OR BORON)
L41         5087 SEA ABB=ON  PLU=ON  INITIAL##(5A)(B OR BORON)
L42         9883 SEA ABB=ON  PLU=ON  BASE(5A)(B OR BORON)
L43         3970 SEA ABB=ON  PLU=ON  SUPPORT(5A)(B OR BORON)
L44          177 SEA ABB=ON  PLU=ON  L36 AND (L39 OR L40 OR L41 OR L42)
                 D L38 ALL HITSTR TOT

     FILE 'STNGUIDE' ENTERED AT 09:13:30 ON 10 MAR 2005

     FILE 'HCAPLUS' ENTERED AT 09:14:36 ON 10 MAR 2005
                 E ATOMIC LAYER DEPOSITION/CT
                 E E4+ALL/CT
L45        15927 SEA ABB=ON  PLU=ON  ("VAPOR PHASE EPITAXY"/CT OR "ATOMIC LAYER
                 EPITAXY"/CT) OR ATOMIC LAYER OR ALD OR ALE
L46        68581 SEA ABB=ON  PLU=ON  MOLECULAR BEAM OR MBE OR L45
L47            3 SEA ABB=ON  PLU=ON  L44 AND L46
                 D ALL HITSTR TOT

     FILE 'STNGUIDE' ENTERED AT 09:16:13 ON 10 MAR 2005

     FILE 'HCAPLUS' ENTERED AT 09:17:46 ON 10 MAR 2005
L48            4 SEA ABB=ON  PLU=ON  L44 AND L20
                 D ALL HITSTR TOT
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     FILE 'STNGUIDE' ENTERED AT 09:17:57 ON 10 MAR 2005

     FILE 'HCAPLUS' ENTERED AT 09:20:35 ON 10 MAR 2005

     FILE 'HCAPLUS' ENTERED AT 09:20:43 ON 10 MAR 2005
L49          285 SEA ABB=ON  PLU=ON  L39 AND (L41 OR L42 OR L43)
L50          206 SEA ABB=ON  PLU=ON  L40 AND (L41 OR L42 OR L43)
L51           62 SEA ABB=ON  PLU=ON  L41 AND (L42 OR L43)
L52           55 SEA ABB=ON  PLU=ON  L42 AND L43
L53            6 SEA ABB=ON  PLU=ON  L44 AND (L49 OR L50 OR L51 OR L52)
                 D ALL HITSTR TOT

     FILE 'STNGUIDE' ENTERED AT 09:21:17 ON 10 MAR 2005

     FILE 'HCAPLUS' ENTERED AT 09:23:44 ON 10 MAR 2005
L54          107 SEA ABB=ON  PLU=ON  (L20 OR L21 OR L22) AND L36
L55          102 SEA ABB=ON  PLU=ON  L54 NOT (L53 OR L48 OR L47 OR L38)
L56            5 SEA ABB=ON  PLU=ON  L55 AND BORON(9W)TUNGSTEN NITRIDE
                 D ALL HITSTR TOT

     FILE 'STNGUIDE' ENTERED AT 09:25:18 ON 10 MAR 2005

     FILE 'HCAPLUS' ENTERED AT 09:27:41 ON 10 MAR 2005
L57         1994 SEA ABB=ON  PLU=ON  ((L17 OR L18) OR (L33 OR L34 OR L35))(L)SUB
                 STRATE
L58        16665 SEA ABB=ON  PLU=ON  ((L17 OR L18) OR (L33 OR L34 OR L35))(L)MOA
                 /RL
L59          640 SEA ABB=ON  PLU=ON  ((L17 OR L18) OR (L33 OR L34 OR L35))(L)PRE
                 CURS#####
L60          129 SEA ABB=ON  PLU=ON  ((L17 OR L18) OR (L33 OR L34 OR L35))(L)STA
                 RT#######
L61           30 SEA ABB=ON  PLU=ON  (L57 OR L58 OR L59 OR L60) AND L20
L62           28 SEA ABB=ON  PLU=ON  L61 NOT (L56 OR L53 OR L48 OR L47 OR L38)
L63            0 SEA ABB=ON  PLU=ON  L62 AND BORON/TI
L64            1 SEA ABB=ON  PLU=ON  L62 AND B/TI
                 D TI
                 D ALL HITSTR
L65           14 SEA ABB=ON  PLU=ON  L20(L)(UPPER##### OR FINAL OR TOP########
                 OR OUTER#### OR EXTERNAL### OR OUTSIDE)
L66            1 SEA ABB=ON  PLU=ON  L62 AND L65
                 D ALL HITSTR
L67           26 SEA ABB=ON  PLU=ON  L62 NOT (L64 OR L66)
                 D ALL HITSTR TOT

     FILE 'STNGUIDE' ENTERED AT 09:33:22 ON 10 MAR 2005

     FILE 'WPIX, JAPIO' ENTERED AT 09:50:34 ON 10 MAR 2005
L68        50208 SEA ABB=ON  PLU=ON  (FIRST OR SUBSTRATE)(4A)(B OR BORON)
L69         1705 SEA ABB=ON  PLU=ON  AFTER(1W)(BORON OR B)
L70         7165 SEA ABB=ON  PLU=ON  THEN(5A)(W OR TUNGSTEN OR WN)
L71            0 SEA ABB=ON  PLU=ON  L68 AND L69 AND L70
L72          123 SEA ABB=ON  PLU=ON  L68 AND L69
L73           39 SEA ABB=ON  PLU=ON  L68 AND L70
L74            2 SEA ABB=ON  PLU=ON  L69 AND L70
                 D MAX 1-2

     FILE 'WPIX, JAPIO' ENTERED AT 09:53:37 ON 10 MAR 2005
L75           17 SEA ABB=ON  PLU=ON  (L72 OR L73) AND FIRST(7A)(B OR BORON) AND
                 SUBSTRATE(7A)(B OR BORON)
L76           17 SEA ABB=ON  PLU=ON  L75 NOT L74

L77         8637 SEA ABB=ON  PLU=ON  (W OR TUNGSTEN)(2A) METAL########
L78         2896 SEA ABB=ON  PLU=ON  WN OR TUNGSTEN(W) NITRIDE
L79            0 SEA ABB=ON  PLU=ON  L76 AND L77 AND L78
L80            1 SEA ABB=ON  PLU=ON  L76 AND L77
L81            1 SEA ABB=ON  PLU=ON  L76 AND L78
L82            2 SEA ABB=ON  PLU=ON  (L80 OR L81)
                 D MAX 1-2
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L83           2 SEA ABB=ON  PLU=ON  BORON AND L76
                D MAX 1-2
L84          18 SEA ABB=ON  PLU=ON  BORON AND (W OR TUNGSTEN) AND WN
                D MAX 1-18

     FILE 'STNGUIDE' ENTERED AT 09:58:00 ON 10 MAR 2005

     FILE 'HCAPLUS' ENTERED AT 10:36:05 ON 10 MAR 2005

     FILE 'HCAPLUS' ENTERED AT 10:36:36 ON 10 MAR 2005
L85           3 SEA ABB=ON  PLU=ON  (BORON OR BORANE OR DIBORANE OR BH OR BH2
                OR BORIDE OR DIBORIDE OR BH4 OR B2H OR B2H4)(5W)("W" OR
                TUNGSTEN)(5W)(WN OR TUNGSTEN NITRIDE)

     FILE 'HCAPLUS' ENTERED AT 10:39:20 ON 10 MAR 2005
L86           2 SEA ABB=ON  PLU=ON  B2H6(5W)("W" OR TUNGSTEN)(5W)(WN OR
                TUNGSTEN NITRIDE)
L87           0 SEA ABB=ON  PLU=ON  L86 NOT L85
L88       11169 SEA ABB=ON  PLU=ON  (ELEMENTAL OR METAL####)(2A)(W OR TUNGSTEN)

L89        6157 SEA ABB=ON  PLU=ON  (NITRID##### OR NITROGEN########)(2A)(W OR
                TUNGSTEN)
L90        2202 SEA ABB=ON  PLU=ON  WN
L91         418 SEA ABB=ON  PLU=ON  L88 AND (L89 OR L90)

     FILE 'HCAPLUS' ENTERED AT 10:42:19 ON 10 MAR 2005
L92      304821 SEA ABB=ON  PLU=ON  (BORON OR BORANE OR DIBORANE OR BH OR BH2
                OR BORIDE OR DIBORIDE OR BH4 OR B2H OR B2H4 OR B2H6 OR
                (GAS#### OR ATOMIC OR PRECURSOR OR VAPOR### OR CONTAIN####)(2A)
                B)
L93          44 SEA ABB=ON  PLU=ON  L91 AND L92
L94           2 SEA ABB=ON  PLU=ON  L93 AND ATOMIC
L95           2 SEA ABB=ON  PLU=ON  L93 AND (MBE OR MOLECULAR OR ALE OR ALD OR
                EPITAX########)
L96           2 SEA ABB=ON  PLU=ON  (L94 OR L95)
```

10mar05 10:08:15 User259284 Session D3112.2

File 2:INSPEC 1969-2005/Feb W4
(c) Institution of Electrical Engineers

Set	Items	Description
S1	54102	CI=B
S2	11130	CI=W EL
S3	94	CI=(W SS(S)N SS)(S)NE=2
S4	475	CI=(W BIN(S)N BIN)(S)NE=2
S5	475	CI=(W BIN(S)N BIN)
S6	553	S3:S5
S7	321	1AND2
S8	11	1AND3
S9	23	1AND6
S10	8	7AND9
S11	618	BORON(2N)(VAPOR?? OR VAPOUR??? OR ATOMIC OR ALE OR ALD OR - GAS????? OR PRECURSOR??)
S12	1	S6 AND S11

10/9/6
DIALOG(R)File 2:INSPEC

5831768 INSPEC Abstract Number: B9803-2550F-065
Title: W-WN/sub x/ as a low-resistance gate material and local interconnect
Author(s): Galewski, C.J.; Sans, C.A.; Gadgil, P.N.; Matthysse, L.D.; Zetterquist, N.
Author Affiliation: Thin Film Div., GENUS, Sunnyvale, CA, USA
Journal: Microelectronic Engineering Conference Title: Microelectron. Eng. (Netherlands) vol.37-38 p.365-72
Publisher: Elsevier,
Publication Date: Nov. 1997 Country of Publication: Netherlands
CODEN: MIENEF ISSN: 0167-9317
SICI: 0167-9317(199711)37/38L.365:RGML;1-P
Material Identity Number: F621-97006
U.S. Copyright Clearance Center Code: 0167-9317/97/$17.00
Conference Title: Second European Workshop on Materials for Advanced Metallization. MAM'97
Conference Sponsor: Int. Union for Vacuum Sci., Tech. & Applications; Minist. Educ. Nat. Enseignement Superieur
Conference Date: 16-19 March 1997 Conference Location: Villard de Lans, France
Document Number: S0167-9317(97)00134-2
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: In this study, we continue a proposal to use in-situ deposition of an interfacial WN/sub x/ film as a process that enables the use of W as a low-resistance gate and local interconnect layer. We have previously found that an interfacial WN/sub x/ layer provides greatly improved adhesion, nucleation, and thermal stability for the subsequent W deposition (Galewski et al., in Adv. Metallization and Interconnect Sys. for ULSI Appl., MRS, 1997). In this work, we extend the scope of the study to investigate the deposition characteristics of the plasma enhanced chemical vapor deposition method in more detail. The variation in film resistivity and its relationship to film morphology is shown to be controlled by the NH/sub 3/-WF/sub 6/ gas flow ratio. The ability to nucleate continuous 10 nm WN/sub x/ films is demonstrated by comparing film thickness and resistivity. The persistebeta-W phase in W films that occur without a nucleation layer of amorphous WN/sub x/ is found to result from a combination of dendritic growth and voids. Impurity dopant diffusion is investigated using secondary ion mass spectroscopy (SIMS). The fact that WN/sub x/ is an effective diffusion barrier to boron and phosphorous, even when deposited directly on silicon damaged by 5*10/sup 15/ cm/sup -2/ implants, suggests its suitability as a contact barrier. The oxidation behaviour of WN/sub x/ was investigated and found to be essentially the same as that of pure W. (16 Refs)
Chemical Indexing:
W-WN int - WN int - N int - W int - WN bin - **N bin** - **W bin** - **W el** (Elements - 1,2,2)
NH3WF6 ss - F6 ss - H3 ss - F ss - H ss - N ss - W ss (Elements - 4)
Si sur - Si el (Elements - 1)
B el (Elements - 1)
P el (Elements - 1)
Numerical Indexing: size 1.0E-08 m

B-implanted Si
WN
W

L67 ANSWER 6 OF 26 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2003:912790 HCAPLUS
DN 139:389741
ED Entered STN: 21 Nov 2003
TI Method for forming multilayer gate structure with decreased contact resistance
IN Chen, Neng-kuo; Yasushi, Akasaka
PI US 2003216020 A1 20031120 US 2003-337293 20030107
TW 546842 B 20030811 TW 2002-91110458 20020517
PRAI TW 2002-91110458 A 20020517
AB The present invention relates to a multilayer gate structure and especially to a multilayer gate structure with lower contact resistance. A multilayer gate structure sequentially formed from a gate oxide layer, a doped Si layer, a SiGe layer, a nitride W layer, and a W layer is described. The polysilicon layer is doped with B. The SiGe layer is formed by deposition or ion implantation process. Because the B migrates more slowly in the SiGe layer, during the thermal process, the B does not migrate to the nitride W layer and thus the contact resistance of the gate structure is maintained at a desired level.
IT **7440-42-8**, Boron, uses
RL: DEV (Device component use); **MOA (Modifier or additive use)**;
USES (Uses)
(Si doped with; method for forming multilayer gate structure with decreased contact resistance)
RN 7440-42-8 HCAPLUS
CN Boron (8CI, 9CI) (CA INDEX NAME)

B-doped Si

B

WN

W

IT **12058-38-7**, Tungsten nitride (WN)
RL: DEV (Device component use); USES (Uses)
(method for forming multilayer gate structure with decreased contact resistance)
RN 12058-38-7 HCAPLUS
CN Tungsten nitride (WN) (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

N≡W

L67 ANSWER 1 OF 26 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2004:893869 HCAPLUS
DN 142:166995
ED Entered STN: 27 Oct 2004
TI Method for forming dual-implanted polysilicon gate of semiconductor device
IN Yeo, In Seok
PA Hynix Semiconductor Inc., S. Korea

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI KR 2001065907	A	20010711	KR 1999-66923	19991230
PRAI KR 1999-66923		19991230		

CLASS
AB A method for forming a dual-implanted polysilicon gate is to ensure the concentration profile of a stable B ion by preventing a dopant depletion and a dopant transmission in a polysilicon layer of a P-channel MOSFET region. A gate insulating layer is grown on a Si substrate. A polysilicon layer is formed on the gate insulating layer. A CoSi2 layer is deposited on the polysilicon layer. The 1st photoresist pattern is formed to coat a P-channel MOSFET region. Phosphorus is implanted into the exposed CoSi2 layer. After removing the 1st photoresist pattern, the 2nd photoresist pattern is formed to coat N-channel MOSFET region. B is implanted into the exposed CoSi2 layer. After removing the 2nd photoresist pattern, the entire structure is annealed to diffuse and activate the ion implanted dopants. After wet etching the CoSi2 layer, a WN layer and a W layer are deposited on the polysilicon layer. A gate electrode pattern is formed by selectively etching the W layer, the WN layer, and the polysilicon layer.

B-doped Si
WN
W

IT **12058-38-7**, Tungsten nitride (WN)
RL: DEV (Device component use); USES (Uses)
(method for forming dual-implanted polysilicon gate of semiconductor device)
RN 12058-38-7 HCAPLUS
CN Tungsten nitride (WN) (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

N≡W

IT **7440-42-8**, Boron, uses
RL: DEV (Device component use); **MOA (Modifier or additive use)**;
USES (Uses)
(silicon doped with; method for forming dual-implanted polysilicon gate of semiconductor device)
RN 7440-42-8 HCAPLUS
CN Boron (8CI, 9CI) (CA INDEX NAME)

B

10/9/3
DIALOG(R)File 2:INSPEC

6671143 INSPEC Abstract Number: B2000-09-2560R-054
Title: A thin amorphous silicon buffer process for suppression of W polymetal gate depletion in PMOS
Author(s): Ohtake, F.; Akasaka, Y.; Murakoshi, A.; Suguro, K.; Nakanishi, T.
Author Affiliation: T Project Group, Fujitsu Labs. Ltd., Japan
Conference Title: 2000 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.00CH37104) p.74-5
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xv+226 pp.
ISBN: 0 7803 6305 1 Material Identity Number: XX-2000-01415
U.S. Copyright Clearance Center Code: 0 7803 6305 1/2000/$10.00
Conference Title: 2000 Symposium on VLSI Technology. Digest of Technical Papers
Conference Date: 13-15 June 2000 Conference Location: Honolulu, HI, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: The mechanism of gate depletion in PMOS W polymetal (W/WN/sub x//poly-Si) gate was investigated. It was found for the first time that the pile-up of boron (B) occurred at the WN/sub x//poly-Si interface due to B-N formation and the B concentration in poly-Si decreased resulting in gate depletion. In order to prevent the B pile-up, we developed a new process module and succeeded in suppressing the gate depletion without B penetration into Si substrate by using a thin amorphous Si buffer (ASB) layer combined with miniaturization of poly-Si grain-size. (2 Refs)
Subfile: B
Descriptors: grain size; MOSFET; semiconductor device metallisation; tungsten
Identifiers: amorphous silicon buffer layer; W polymetal gate depletion; PMOS transistor; boron pile-up; grain size; W-WN-Si:B; Si
Class Codes: B2560R (Insulated gate field effect transistors); B2550F (Metallisation and interconnection technology)
Chemical Indexing:
W-WN-Si:**B** int - Si:**B** int - Si int - WN int - **B** int - N int - W int - Si:**B** bin - Si bin - WN bin - **B** bin - **N bin** - **W bin** - Si el - **B** el - **W el** - **B** dop (Elements - 1,**2**,1,1,**2**,4)
Si int - Si el (Elements - 1)

B- implanted Si
WN / W

L84 ANSWER 9 OF 18 WPIX COPYRIGHT 2005 THE THOMSON CORP on STN
AN 2002-486872 [52] WPIX
DNC C2002-138225
TI Transistor manufacture.
DC L03 U11
IN MO, G G
PA (HYNI-N) HYNIX SEMICONDUCTOR INC
CYC 1
PI KR 2002002699 A 20020110 (200252)* 1 H01L021-8232
ADT KR 2002002699 A KR 2000-36951 20000630
PRAI KR 2000-36951 20000630
IC ICM H01L021-8232
AB KR2002002699 A UPAB: 20020815
NOVELTY - A method for manufacturing a transistor is provided to prevent a short channel effect of **boron** ions in a channel region in a selective oxide process and to prevent a pin hole, by forming a gate electrode after NH3 annealing process is performed while a polycrystalline silicon layer, a **WN** layer as a barrier layer and a **tungsten** layer are stacked.

DETAILED DESCRIPTION - The gate insulation layer(32), the polycrystalline silicon layer(33), the **WN** layer(34) and the **tungsten** layer(35) are sequentially formed on a substrate(31). An annealing process is performed in a NH3 atmosphere(36). A hard mask layer is formed on the **tungsten** layer. The hard mask layer, the **tungsten** layer, the **WN** layer and the polycrystalline silicon layer are selectively etched to form the gate electrode. The gate electrode is selectively oxidized.

Dwg.1/10
FS CPI EPI
FA AB; GI
MC CPI: L04-C16A; L04-E01A
EPI: U11-C03J2; U11-C03J2A; U11-C18A3

L67 ANSWER 16 OF 26 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2002:533966 HCAPLUS
DN 137:102408
ED Entered STN: 17 Jul 2002
TI Low dielectric constant nanotube film for semiconductor device fabrication using the damascene process
IN Yang, Cheng-jer; Tan-Tai, Fu-kuo; Cheng, Huang-chung
PA Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01J009-02
ICS B32B009-00
NCL 430311000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

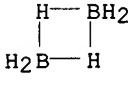
PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6420092	B1	20020716	US 1999-417331	19991013
PRAI TW 1999-88111924	A	19990714		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
US 6420092	ICM	H01J009-02
	ICS	B32B009-00
	NCL	430311000
US 6420092	ECLA	H01L021/318

AB A low dielec. constant nanotube, which can be used in the damascene process, and the fabrication method for a nonselective and a selective nanotube thin film layer are described. The nonselective deposition of the nanotube thin film layer includes forming a catalytic layer on the substrate followed by chemical vapor depositing a nanotube thin film layer on the catalytic layer. The selective deposition of the nanotube thin film layer includes forming a catalytic layer on the substrate followed by patterning the catalytic layer. A patterned photoresist layer can also form on the substrate, followed by forming multiple of catalytic layers on the photoresist layer and on the exposed substrate resp. The photoresist layer and the overlying catalytic layer are removed. Thereafter, a nanotube layer is formed on the patterned catalytic layer by CVD. A conformal barrier layer can further form on the substrate followed by filling the openings of the nanotube on the substrate with a metal conductive layer and conducting a damascene process.

IT **19287-45-7**, Diborane
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(boron nitride nanotube **precursor**; low dielec. constant nanotube film for semiconductor device fabrication using damascene process)
RN 19287-45-7 HCAPLUS
CN Diborane(6) (8CI, 9CI) (CA INDEX NAME)



IT **12058-38-7**, Tungsten mononitride
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(low dielec. constant nanotube film for semiconductor device fabrication using damascene process with)
RN 12058-38-7 HCAPLUS
CN Tungsten nitride (WN) (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

L67 ANSWER 20 OF 26 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2000:304343 HCAPLUS
DN 132:302036
ED Entered STN: 10 May 2000
TI Stacked gate structure for flash memory application and fabrication
IN Huang, Richard J.
PA Advanced Micro Devices, Inc., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-8247
ICS H01L029-788; H01L029-76; H01L029-94
NCL 257315000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6060741	A	20000509	US 1998-154072	19980916
PRAI US 1998-154072		19980916		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
US 6060741	ICM	H01L021-8247
	ICS	H01L029-788; H01L029-76; H01L029-94
	NCL	257315000
US 6060741	ECLA	H01L029/423D2B2

AB To form a low resistance gate for use in a flash EPROM or EEPROM, a B doped amorphous Si layer is formed on an oxide layer and a layer of W nitride formed thereon. A layer of W silicide is then formed on the W nitride layer acts as a barrier preventing out diffusion of a contaminating dopant, e.g., B, and exhibits good adhesion to the amorphous Si layer. The W silicide layer, in turn, exhibits good adhesion to the W nitride layer thereby preventing lifting of the silicide layer and dopant penetration.

IT **264263-54-9**, Tungsten nitride (WN2-3)
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in stacked gate structure for flash memory application and fabrication)
RN 264263-54-9 HCAPLUS
CN Tungsten nitride (WN2-3) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	2 - 3	17778-88-0
W	1	7440-33-7

IT **7440-42-8**, Boron, uses
RL: **MOA (Modifier or additive use)**; USES (Uses)
(stacked gate structure for flash memory application and fabrication using boron doped silicon amorphous films)
RN 7440-42-8 HCAPLUS
CN Boron (8CI, 9CI) (CA INDEX NAME)

B

L67 ANSWER 8 OF 26 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2003:862846 HCAPLUS
DN 139:344335
ED Entered STN: 04 Nov 2003
TI Metal gate with PVD amorphous silicon layer and barrier layer for CMOS devices, and method of making with a replacement gate process
IN Besser, Paul R.; Xiang, Qi; Buynoski, Matthew S.
PA Advanced Micro Devices, Inc., USA
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6642590	B1	20031104	US 2000-691227	20001019
PRAI	US 2000-691227		20001019		

AB The present invention relates to the field of semiconductor processing, and more particularly, to the formation of metallic gate electrodes using the replacement gate process technique. The gate includes a high dielec. constant on the substrate, and a phys. vapor deposited (PVD) layer of amorphous Si on the high k gate dielec. A barrier layer is deposited on the PVD amorphous Si layer. The metal is then formed on the barrier layer. The work function of the metal gate is substantially the same as a polysilicon gate due to the presence of the PVD amorphous Si layer. The barrier layer prevents interaction between the PVD amorphous Si layer and the metal, thereby allowing higher temperature subsequent processing while preserving the work function of the gate.
IT **12058-38-7**, Tungsten nitride (WN)
RL: DEV (Device component use); USES (Uses)
(diffusion barrier; metal gate with PVD amorphous silicon layer and barrier layer for CMOS devices, and method of making with a replacement gate process)
RN 12058-38-7 HCAPLUS
CN Tungsten nitride (WN) (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

N≡W

IT **7440-42-8**, Boron, uses
RL: DEV (Device component use); **MOA (Modifier or additive use)**; USES (Uses)
(semiconductor material doped with; metal gate with PVD amorphous silicon layer and barrier layer for CMOS devices, and method of making with a replacement gate process)
RN 7440-42-8 HCAPLUS
CN Boron (8CI, 9CI) (CA INDEX NAME)

B

L67 ANSWER 13 OF 26 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2002:849964 HCAPLUS
DN 137:361376
ED Entered STN: 08 Nov 2002
TI Modification to fill layers for inlaying semiconductor patterns
IN Laursen, Thomas
PA Speedfam-Ipec Corporation, USA
SO PCT Int. Appl., 18 pp.
CODEN: PIXXD2
DT Patent
LA English
IC ICM H01L
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002089181	A2	20021107	WO 2001-US51639	20011026
	WO 2002089181	A3	20030807		
	US 6521537	B1	20030218	US 2000-703210	20001031
PRAI	US 2000-703210	A	20001031		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
WO 2002089181	ICM	H01L

AB The invention provides a method of fabricating semiconductor chips that includes modifying phys. properties of selected deposited fill layers over patterns having up-features and down-features, with fill to be retained in down-features. The modification enhances chemical mech. polishing rates, or other polishing, of the modified fill layers to reduce dishing of fill material and achieves this without substantially affecting the elec. properties of the final semiconductor chip product. The invention also provides intermediate chip products and final chip products of the method

IT **12058-38-7**, Tungsten nitride (WN)
RL: DEV (Device component use); USES (Uses)
(diffusion barrier; modification to fill layers for inlaying semiconductor patterns)
RN 12058-38-7 HCAPLUS
CN Tungsten nitride (WN) (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

N≡W

IT **7440-42-8**, Boron, uses
RL: DEV (Device component use); **MOA (Modifier or additive use)**;
USES (Uses)
(multilayer stack additive; modification to fill layers for inlaying semiconductor patterns)
RN 7440-42-8 HCAPLUS
CN Boron (8CI, 9CI) (CA INDEX NAME)

B

L67 ANSWER 3 OF 26 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2004:533504 HCAPLUS
DN 141:97827
ED Entered STN: 02 Jul 2004
TI Semiconductor device and method for manufacturing same
IN Makita, Naoki
PA Sharp Kabushiki Kaisha, Japan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2004124469	A1	20040701	US 2003-734312	20031215
	JP 2004207298	A2	20040722	JP 2002-371422	20021224
PRAI	JP 2002-371422	A	20021224		

AB A semiconductor device includes a thin-film transistor including a semiconductor layer that includes a channel region, a source region and a drain region, a gate insulating film provided on the semiconductor layer, and a gate electrode for controlling the conductivity of the channel region, wherein the surface of the semiconductor layer includes a minute protruding portion, and the side surface inclination angle of the gate electrode is larger than the inclination angle of the protruding portion of the semiconductor layer.

IT **12058-38-7**, Tungsten nitride (WN)
RL: DEV (Device component use); USES (Uses)
(semiconductor device and manufacture of same)
RN 12058-38-7 HCAPLUS
CN Tungsten nitride (WN) (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

N≡W

IT **7440-42-8**, Boron, uses
RL: **MOA (Modifier or additive use)**; USES (Uses)
(semiconductor device and manufacture of same)
RN 7440-42-8 HCAPLUS
CN Boron (8CI, 9CI) (CA INDEX NAME)

B

L67 ANSWER 2 OF 26 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2004:645816 HCAPLUS
DN 141:183047
ED Entered STN: 11 Aug 2004
TI Semiconductor device structure having alignment marks with shallow trench isolation
IN Ramkumar, Krishnaswamy; Sadoughi, Sharmin
PA Cypress Semiconductor Corporation, USA
PI US 6774452 B1 20040810 US 2002-321965 20021217
PRAI US 2002-321965 20021217
AB A semiconductor device structure including a semiconductor substrate, an isolation trench in the semiconductor substrate, and an alignment trench in the semiconductor substrate is disclosed. The structure also includes a dielec. layer and a metallic layer. The dielec. layer is on the semiconductor substrate and in both the isolation trench and the alignment trench. The dielec. layer fills the isolation trench and does not fill the alignment trench. The metallic layer is on the dielec. layer.
IT **12058-38-7**, Tungsten nitride (WN)
RL: DEV (Device component use); USES (Uses)
(semiconductor device structure having alignment marks with shallow trench isolation)
RN 12058-38-7 HCAPLUS
CN Tungsten nitride (WN) (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

N≡W

IT **7440-42-8**, Boron, uses
RL: **MOA (Modifier or additive use)**; USES (Uses)
(semiconductor device structure having alignment marks with shallow trench isolation)
RN 7440-42-8 HCAPLUS
CN Boron (8CI, 9CI) (CA INDEX NAME)

B

L85 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2001:40280 HCAPLUS
DN 134:79023
ED Entered STN: 17 Jan 2001
TI CVD of tungsten film on tungsten nitride film, semiconductor device, and CVD apparatus
IN Kitazaki, Masaki; Nishina, Kazuhiro
PA Applied Materials, Inc., USA
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM C23C016-02
ICS C23C016-14; C23C016-34; H01L021-28; H01L021-285
CC 75-1 (Crystallography and Liquid Crystals)
Section cross-reference(s): 76
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001011627	A2	20010116	JP 1999-174227	19990621
PRAI JP 1999-174227		19990621		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
JP 2001011627	ICM	C23C016-02
	ICS	C23C016-14; C23C016-34; H01L021-28; H01L021-285

AB The title method involves spraying a B2H6 gas onto a substrate having a tungsten nitride film in a vacuum chamber, evacuating the chamber, forming a W nucleation film on the substrate by a CVD method, and carrying out CVD of a W film using the nucleation film. A semiconductor device having the above W film is also described. An apparatus is also described, for forming the nucleation film using WF6, SiH4, and B2H6.

L85 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2001:40281 HCAPLUS
DN 134:79024
ED Entered STN: 17 Jan 2001
TI CVD of tungsten film on tungsten nitride film, semiconductor device, and CVD apparatus
IN Kitazaki, Masaki; Nishina, Kazuhiro
PA Applied Materials, Inc., USA
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM C23C016-02
ICS C23C016-14; C23C016-34; H01L021-285
CC 75-1 (Crystallography and Liquid Crystals)
Section cross-reference(s): 76

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001011629	A2	20010116	JP 1999-174260	19990621
PRAI JP 1999-174260		19990621		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
JP 2001011629	ICM	C23C016-02
	ICS	C23C016-14; C23C016-34; H01L021-285

AB The title method involves spraying a SiH4 gas and then a B2H6 gas onto a substrate having a tungsten nitride film in a vacuum chamber, evacuating the chamber, forming a W nucleation film on the substrate by a CVD method, and carrying out CVD of a W film using the nucleation film. A semiconductor device having the above W film is also described. An apparatus is also described, for forming the nucleation film using WF6, SiH4, and B2H6.

L96 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2001:284166 HCAPLUS
DN 134:303342
ED Entered STN: 20 Apr 2001
TI Method of depositing transition metal nitride thin films
IN Elers, Kai-Erik; Haukka, Suvi Paeivikki; Saanila, Ville Antero; Kaipio, Sari Johanna; Soininen, Pekka Juha
PA ASM Microchemistry Oy, Finland

PI	WO 2001027347	A1	20010419	WO 2000-FI895	20001013
	FI 9902234	A	20010416	FI 1999-2234	19991015
	TW 541351	B	20030711	TW 2000-89121352	20001012
	EP 1242647	A1	20020925	EP 2000-969596	20001013
	EP 1242647	B1	20030813		
	JP 2003511561	T2	20030325	JP 2001-529476	20001013
	US 6863727	B1	20050308	US 2002-110730	20020411
	US 2002187256	A1	20021212	US 2002-210715	20020730
	US 6821889	B2	20041123		
	US 2003031807	A1	20030213	US 2002-246131	20020917
	US 6800552	B2	20041005		
PRAI	FI 1999-2234	A	19991015		
	FI 1999-2233	A	19991015		
	FI 1999-2235	A	19991015		
	US 1999-159799P	P	19991015		
	US 2000-176948P	P	20000118		
	FI 2000-564	A	20000310		
	US 2000-687204	A1	20001013		
	US 2000-687205	A1	20001013		
	WO 2000-FI895	W	20001013		

OS MARPAT 134:303342
AB This invention concerns a method for depositing transition metal nitride thin films by an **at.** layer deposition (**ALD**) type process. According to the method vapor-phase pulses of a metal source material, a reducing agent capable of reducing metal source material, and a nitrogen source material capable of reacting with the reduced metal source material are alternately and sequentially fed into a reaction space and contacted with the substrate. According to the invention as the reducing agent is used a **boron** compound which is capable of forming gaseous reaction byproducts when reacting with the metal source material.
IT **Boranes**
Carboranes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(method of depositing transition metal nitride films by **ALD** using reducing agent of)
IT 37359-53-8, **Tungsten nitride**
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(method of depositing transition metal nitride films by **ALD**)

L67 ANSWER 11 OF 26 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2003:174419 HCAPLUS
DN 138:197183
ED Entered STN: 07 Mar 2003
TI Method for semiconductor gate doping using laser thermal processing
IN Seibel, Cindy; Talwar, Somit
PA Ultratech Stepper, Inc., USA

PI	US 2003045074	A1	20030306	US 2001-941817	20010829
	US 6777317	B2	20040817		
	WO 2003021640	A2	20030313	WO 2002-US26362	20020815
	WO 2003021640	A3	20030417		
	EP 1421605	A2	20040526	EP 2002-757231	20020815
	JP 2005502203	T2	20050120	JP 2003-525888	20020815
PRAI	US 2001-941817	A	20010829		
	WO 2002-US26362	W	20020815		

AB The invention relates to a method for doping a polycryst. silicon gate in a metal-oxide-semiconductor (MOS) device using laser thermal processing. The method includes forming an insulation layer on a top surface of a crystalline silicon substrate. Next, an amorphous silicon layer is formed on top of and in contact with the insulation layer, and then a dopant is introduced into the top surface layer of the amorphous silicon layer. The top surface of the amorphous silicon layer is irradiated with a laser beam and the heat of the radiation causes the top surface layer to melt and initiates explosive recrystn. (XRC) of the amorphous silicon layer. The XRC process transforms the amorphous silicon layer into a polycryst. silicon gate and distributes the dopant homogeneously throughout the polycryst. gate.

IT **12058-38-7**, Tungsten nitride (WN)
RL: DEV (Device component use); USES (Uses)
(contact material; method for semiconductor gate doping using laser thermal processing)
RN 12058-38-7 HCAPLUS
CN Tungsten nitride (WN) (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

N≡W

IT **7440-42-8**, Boron, processes
RL: **MOA (Modifier or additive use)**; PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(dopant; method for semiconductor gate doping using laser thermal processing)
RN 7440-42-8 HCAPLUS
CN Boron (8CI, 9CI) (CA INDEX NAME)

B

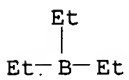
L67 ANSWER 9 OF 26 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2003:242540 HCAPLUS
DN 138:258761
ED Entered STN: 28 Mar 2003
TI Atomic layer deposition of metal or hard metal compound films controlled by a reduction pulse
IN Elers, Kai Erik; Li, Wei-Min
PA ASM America, Inc., USA; ASM Microchemistry Oy

PI	WO 2003025243	A2	20030327	WO 2002-US29032	20020910
	WO 2003025243	A3	20031127		
	EP 1425435	A2	20040609	EP 2002-798955	20020910
	JP 2005503484	T2	20050203	JP 2003-530012	20020910
	US 2003082296	A1	20030501	US 2002-242368	20020912
	TW 559890	B	20031101	TW 2002-91120831	20020912
PRAI	US 2001-322385P	P	20010914		
	WO 2002-US29032	W	20020910		

AB Conformal metal or hard metal-compound films are applied on substrates by cyclic atomic-layer deposition process with alternating pulses of reactants. The chemical-vapor deposition cycle includes a metal halide reactant and a 2nd reactant with a species to be included in the film, and later a 3rd reactant capable of gettering residual halides from the monolayer deposit. The chemical-vapor deposition is suitable for growing the films of transition metal, nitride, carbide, and/or carbonitride, with the associated decrease in the amount of corrosive chemical compound (especially H halides) during the deposition on metal or oxide substrates at nominally 225-400°. The getter compds. protect the substrate surfaces sensitive to H halides and NH4 halides (especially Al, Cu, and/or SiO2) against corrosion. The process is suitable for nanolaminate structures incorporating metal films, especially for elec.-circuit applications to form a diffusion barrier <20 nm thick. The complex film applied by cyclic deposition is optionally W carbonitride applied using controlled cyclic flow of WF6, NH3, and triethylboron.

IT **12058-38-7**, Tungsten nitride (WN)
RL: PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process)
(film, deposition of; atomic layer deposition of metal or hard compound films controlled by reduction pulse)
RN 12058-38-7 HCAPLUS
CN Tungsten nitride (WN) (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

IT **97-94-9**, Triethylboron
RL: **MOA (Modifier or additive use)**; USES (Uses)
(vapor-deposition system with, for films; atomic layer deposition of metal or hard compound films controlled by reduction pulse)
RN 97-94-9 HCAPLUS
CN Borane, triethyl- (8CI, 9CI) (CA INDEX NAME)



L67 ANSWER 7 OF 26 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2003:912483 HCAPLUS
DN 139:389799
ED Entered STN: 21 Nov 2003
TI Design and fabrication of an MIS capacitor
IN Basceri, Cem; Derderian, Garo J.

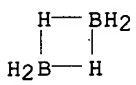
	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003213987	A1	20031120	US 2002-145993	20020516
	US 2004046197	A1	20040311	US 2003-659435	20030911
PRAI	US 2002-145993	A3	20020516		

AB An MIS capacitor with low leakage and high capacitance is disclosed. A layer of hemispherical grained polysilicon (HSG) is formed as a lower electrode. Prior to the dielec. formation, the hemispherical grained polysilicon layer may be optionally subjected to a nitridization or anneal process. A dielec. layer of Al2O3, or a composite stack of interleaved layers of Al oxide and other metal oxide dielec. materials, is fabricated over the hemispherical grained polysilicon layer and after the optional nitridization or anneal process. The dielec. layer of Al2O3 or the Al oxide composite stack may be optionally subjected to a post-deposition treatment to further increase the capacitance and decrease the leakage current. A metal nitride upper electrode is formed over the dielec. layer or the composite stack by a deposition technique or by atomic layer deposition.

IT **7440-42-8**, Boron, uses
RL: DEV (Device component use); **MOA (Modifier or additive use)**; USES (Uses)
(TiN and WN doped with; design and fabrication of an MIS capacitor)
RN 7440-42-8 HCAPLUS
CN Boron (8CI, 9CI) (CA INDEX NAME)

B

IT **19287-45-7**, Diborane
RL: **MOA (Modifier or additive use)**; PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(dopant source; design and fabrication of an MIS capacitor)
RN 19287-45-7 HCAPLUS
CN Diborane(6) (8CI, 9CI) (CA INDEX NAME)



IT **12058-38-7**, Tungsten nitride (WN)
RL: DEV (Device component use); USES (Uses)
(optionally B doped, capacitor electrode; design and fabrication of an MIS capacitor)
RN 12058-38-7 HCAPLUS
CN Tungsten nitride (WN) (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

L67 ANSWER 4 OF 26 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2004:60729 HCAPLUS
DN 140:121048
ED Entered STN: 26 Jan 2004
TI Method of film deposition using activated precursor gases
IN Chung, Hua; Ku, Vincent W.; Chen, Ling
PA Applied Materials, Inc., USA

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2004007792	A2	20040122	WO 2003-US19706	20030623
	WO 2004007792	A3	20040429		
	W: CN, JP, KR				
	US 2004018304	A1	20040129	US 2002-193574	20020710
	US 6838125	B2	20050104		
PRAI	US 2002-193574	A	20020710		

AB The present invention generally relates to methods of film deposition and, more particularly to methods of film deposition in which precursor gases are activated prior to cyclical introduction to a substrate. In 1 aspect, the method includes providing a metal-containing precursor to an activation zone, and activating the metal-containing precursor to form an activated precursor. The activated precursor gas is transported to a reaction chamber, and a film is deposited on the substrate using a cyclical deposition process, in which the activated precursor gas and a reducing gas are alternately adsorbed on the substrate. Also provided is a method of depositing a film on a substrate using an activated reducing gas. The films formed by the vapor deposition method are suitable for use in integrated circuit fabrication.

IT **12058-38-7P**, Tungsten nitride (WN)
RL: PNU (Preparation, unclassified); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(vapor deposition of; method of film deposition using activated precursor gases)
RN 12058-38-7 HCAPLUS
CN Tungsten nitride (WN) (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

IT **13283-31-3**, Borane, processes **19287-45-7**, DiBorane
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(vapor deposition reducing gas; method of film deposition using activated **precursor** gases)
RN 13283-31-3 HCAPLUS
CN Borane (7CI, 8CI, 9CI) (CA INDEX NAME)

RN 19287-45-7 HCAPLUS
CN Diborane(6) (8CI, 9CI) (CA INDEX NAME)